A 45nm CMOS Technology Exploring low power and Fast 4 bit Full Adder using XOR/XNOR Gates

Base paper Abstract:

In this paper, novel circuits for XOR/XNOR and simultaneous XOR–XNOR functions are proposed. The proposed circuits are highly optimized in terms of the power consumption and delay, which are due to low output capacitance and low short-circuit power dissipation. We also propose six new hybrid 1-bit full-adder (FA) circuits based on the novel full-swing XOR–XNOR or XOR/XNOR gates. Each of the proposed circuits has its own merits in terms of speed, power consumption, power delay product (PDP), driving ability, and so on. To investigate the performance of the proposed designs, extensive HSPICE and Cadence Virtuoso simulations are performed. The simulation results, based on the 65-nm CMOS process technology model, indicate that the proposed designs have superior speed and power against other FA designs. A new transistor sizing method is presented to optimize the PDP of the circuits. In the proposed method, the numerical computation particle swarm optimization algorithm is used to achieve the desired value for optimum PDP with fewer iterations. The proposed circuits are investigated in terms of variations of the supply and threshold voltages, output capacitance, input noise immunity, and the size of transistors.

Enhancement of this Project:

- In this project we proposed 4 bit full adder using 45nm CMOS technology and compare with 65nm COMS technology.
- Also comparing the area, power and speed.

Proposed Abstract:

This paper, explores 4 bit full adder using XOR/XNOR or simultaneous XOR-XNOR gates and also consuming power and area of the circuit and increasing speed. This paper propose 4 bit full adder using full swing XOR/XNOR gates. The existing system simulated in 65nm CMOS technology and using hybrid 1 bit full adder. So it consumes more power for implementation. The proposed circuits simulation results based on 45nm CMOS technology model, it have superior speed and reducing area, power consumption and this circuit has high speed, low power using power delay product (PDP). In the proposed method, the numerical computation particle swarm optimization algorithm is used to achieve the desired value for

optimum PDP with less iteration. In the proposed circuits new transistor sizing is implemented to optimize the PDP circuits. The proposed architecture results are compared with area, power and speed of the existing architecture.

Existing system:

Hybrid FAs are made of two modules, including 2-inputXOR/XNOR (or simultaneous XOR–XNOR) gate and 2-to-1 multiplexer (2-1-MUX) gate. The XOR/XNOR gate is the major consumer of power in the FA cell. Therefore, the power consumption of the FA cell can be reduced by optimum designing of the XOR/XNOR gate. The XOR/XNOR gate has also many applications in digital circuits design. Many circuits have been proposed to implement XOR/XNOR gate, which a few examples of the most efficient ones are shown in Fig. 1(a) shows the full-swing XOR/XNOR gate circuit designed by double pass-transistor logic (DPL) style. This structure has eight transistors. The main problem of this circuit is using two high power consumption NOT gates on the critical path of the circuit, because the NOT gates must drive the output capacitance. Therefore, the size of the transistors in the NOT gates should be increased to obtain lower critical path delay. Furthermore, it causes the creation of an intermediate node with a large capacitance. Of course, this means that the NOT gates drives the output of circuit through, for example, pass transistor or TG. Therefore, the short-circuit power and, thus, the total power dissipation of this circuit are widely increased. Moreover, in the optimum PDP situation, the critical path delay will also be increased slightly

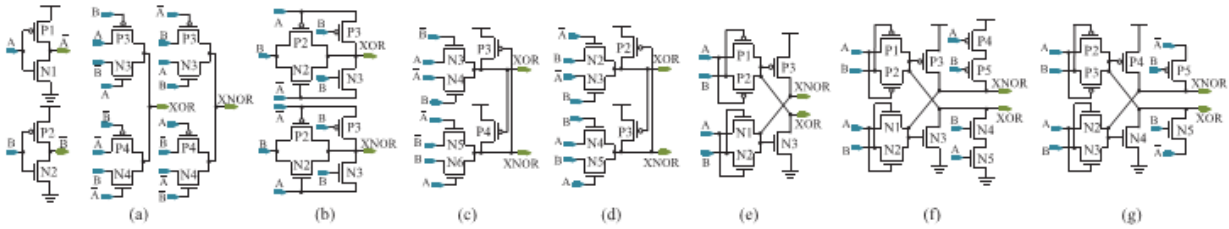

Figure 1 : (a) and (b) Full-swing XOR/XNOR and (c)–(g) XOR–XNOR circuits

Disadvantages:

- More power consumption.
- More Critical Path delay.

Proposed system:

The non full-swing XOR/XNOR circuit of Fig. 2(a) is efficient in terms of the power and delay. Furthermore, this structure has an output voltage drop problem for only one input logical value. To solve this problem and provide an optimum structure for the XOR/XNOR gate, we propose the circuit shown in Fig. 2(b). For all possible input combinations, the output of this structure is full swing. The proposed system have XOR/XNOR gate does not have NOT gates on the critical path of the circuit. Thus, it will have the lower delay and good driving capability in comparison with the structures of Fig. 1(a) and (b). Although the proposed XOR/XNOR gate has one more transistor than the structure of Fig. 1(b), it demonstrates lower power dissipation and higher speed. The input A and B capacitances of the XOR circuit shown in Fig. 2(b) are not symmetric, because one of these two should be connected to the input of NOT gates and another should be connected to the diffusion of n MOS transistor.

Fig. 2. (a) Non full-swing XOR/XNOR gate . (b) Proposed full-swing XOR/XNOR gate. (c) RC model of proposed XOR for AB=10. (d) RC model of proposed XOR for AB=11. (e) Proposed

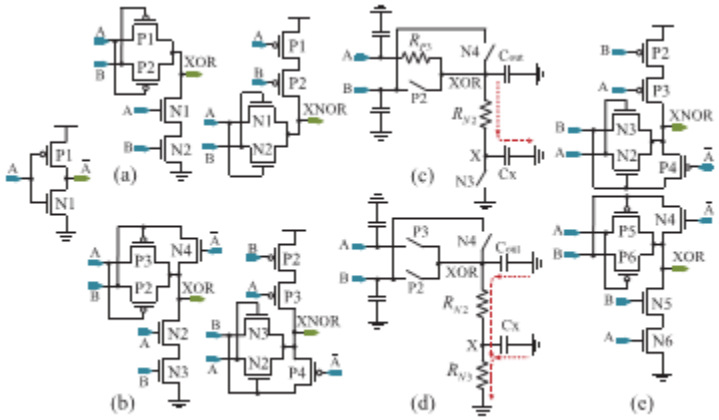

Figure 2. (a) Non full-swing XOR/XNOR gate . (b) Proposed full-swing XOR/XNOR gate. (c) RC model of proposed XOR for AB=10. (d) RC model of proposed XOR for AB=11. (e) Proposed XOR–XNOR gate.

Furthermore, the input capacitances of transistors N2and N3 are not equal in the optimal situation (minimum PDP).Also, the order of input connections to transistors N2 and N3 will not affect the function of the circuit. Thus, it is better to connect the input A, which is also connected to the NOT gates, to the transistor with smaller input capacitance. By doing this, the input capacitances are more symmetrical, and thus, the delay and power consumption of the circuit will be reduced. To clarify which transistor (N2orN3) has larger input capacitance, let us consider the condition that the inputs change from AB=00 to AB=10. In this condition, as the RC model of XOR is shown in Fig. 2(c) and (d), the transistor N2 is driving only the capacitance of node X from GND to $V_{DD} - V_{th_n}$ [Fig. 2(c)], so it will not require lower RN2.But,when the inputs change from AB=10 to AB=11, according to Fig. 2(d), we have

$$k_{N2} = \frac{W_{N2}}{W_{min}}, k_{N3} = \frac{W_{N3}}{W_{min}}, \dots\dots\dots, k_{P3} = \frac{W_{P3}}{W_{min}}$$

$$R_{N2} = \frac{R_{min}}{k_{N2}}, R_{N3} = \frac{R_{min}}{k_{N3}}, a = k_{N4} + k_{P2} + k_{P3}$$

$$C_x = C_{d_{min}} \times k_{N2} + C_{d_{min}} \times k_{N3} = C_{d_{min}} (k_{N2} + k_{N3})$$

$$C_{out} = C_{d_{N4}} + C_{d_{P3}} + C_{d_{min}} \times k_{N2}$$

$$C_{out} = a \times C_{d_{min}} + C_{d_{min}} \times k_{N2} = C_{d_{min}} (a + k_{N2}) \qquad (1)$$

Where W_{min} is the minimum transistor width, R_{min} is the ON-state resistance for the nMOS transistor with W_{min}, $C_{d_{min}}$ is the diffusion capacitance of the transistor, and a is the total size of the transistors P2, P3, andN4.

The Elmore delay ($T_{d_{AB=10\rightarrow11}}$) of Fig. 2(c) and (d) is equal to

$$T_{d_{AB=10\rightarrow11}} = C_{out}\left(\frac{R_{min}}{k_{N2}} + \frac{R_{min}}{k_{N3}}\right) + C_x\left(\frac{R_{min}}{k_{N3}}\right)$$

$$= C_{d_{min}} R_{min}\left[a\left(\frac{1}{k_{N2}} + \frac{1}{k_{N3}}\right) + 2\left(1 + \frac{k_{N2}}{k_{N3}}\right)\right] \qquad (2)$$

now, the average dynamic power dissipation (for the condition that the inputs change from AB=10 to AB=11) can be written as

$$P_{AB=10\rightarrow11} = C_{total} {V_{DD}}^2$$
$$= \left(C_{d_{min}} (k_{N2} + k_{N3}) + C_{d_{min}} (a + k_{N2}) k_{N3} C_{g_{min}} + k_{P2} C_{d_{min}} + k_{P3} C_{g_{min}} + k_{N4} C_{d_{min}}\right) {V_{DD}}^2 \qquad (3)$$

$C_{g_{min}}$ is the gate capacitance of the transistor, and C_{total} is all capacitances that are switched. By assuming $C_{d_{min}} \approx C_{g_{min}} = C$ and a=3 (the size of transistors P2,P3, and N4 equal to the W_{min}

$$P_{AB=10\rightarrow11} = \left((k_{N2} + k_{N3})C + (3 + k_{N2})C + k_{N3}C + 3C\right) {V_{DD}}^2$$

$$= C {V_{DD}}^2 (2k_{N2} + 2k_{N3} + 6) \qquad (4)$$

Finally, by having the value of delay and power dissipation, the PDP of the circuit can be obtained. For a better comparison, the normalized PDP (PDP_n) is considered

$$PDP_n = \frac{T_{d_{AB=10\to11}} \times P_{AB=10\to11}}{CR_{min} \times {CV_{DD}}^2}$$

$$= \left[3\left(\frac{1}{k_{N2}} + \frac{1}{k_{N3}}\right) + 2\left(1 + \frac{k_{N2}}{k_{N3}}\right)\right](2k_{N2} + 2k_{N3} + 6) \qquad (5)$$

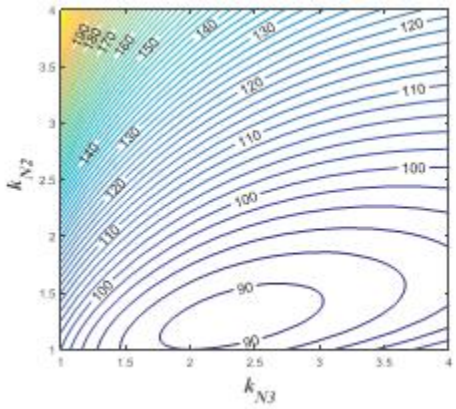

Figure 3.Normalized PDP with a=3for1≤kN2, kN3≤4

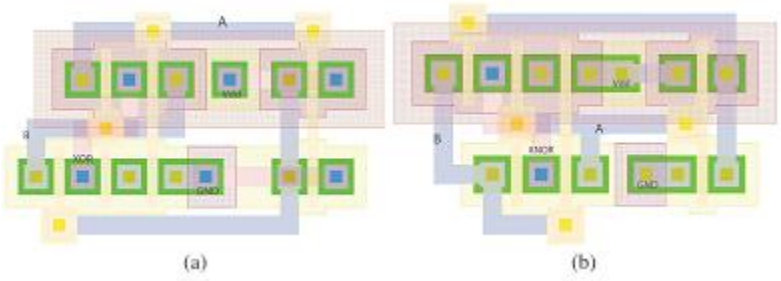

Figure 4. (a) Circuit layout of proposed XOR. (b) Circuit layout of proposed XNOR

Fig. 3 shows the value of normalized PDP with a =3 for 1 ≤kN2, kN3 ≤4. Fig. 3 also shows that, in the optimal condition, the value of kN3is bigger than that of kN2. Therefore, the W/L ratio of the transistor N3 is larger than that of the transistor N2. Thus, the input capacitance of transistor N3 is higher than that of transistorN2 and, to obtain the optimal circuit, it is better to connect input A to the transistor N2. The advantages of the proposed XOR/XNOR circuits are full-swing output, good driving capability, smaller number of interconnecting wires, and straightforward circuit layout. Fig. 4(a) and (b) shows the circuit layout of the proposed XOR and XNOR gates, respectively, designed for minimum power consumption .

Advantages:

- Circuit has very good speed, accuracy, and convergence.
- Less critical path delay.
- It has superior speed and power against other FA designs.

Software Implementation:

- Tanner EDA

Literature survey:

- **N. S. Kim et al., "Leakage current: Moore's law meets static power," Computer**-power consumption is now the major technical problem facing the semiconductor industry. In comments on this problem at the 2002 International Electron Devices Meeting, Intel chairman Andrew Grove cited off-state current leakage in particular as a limiting factor in future microprocessor integration.1 Off-state leakage is static power, current that leaks through transistors even when they are turned off. It is one of two principal sources of power dissipation in today's microprocessors. The other is dynamic power, which arises from the repeated capacitance charge and discharge on the output of the hundreds of millions of gates in today's chips. Until very recently, only dynamic power has been a significant source of power consumption, and Moore's law has helped to control it. Shrinking processor technology has allowed and, below 100 nanometers, actually required reducing the supply voltage. Dynamic power is proportional to the square of supply voltage, so reducing the voltage significantly reduces power consumption. Unfortunately, smaller geometries exacerbate leakage, so static power begins to dominate the power consumption equation in microprocessor design.
- **Low Power Full Adder Using 8T Structure Amin Bazzazi, Member, IAENG, Alireza Mahini and Jelveh Jelin**i-A low power and high performance 1-bit full adder cell is proposed. The 8T Full Adder technique has been used for the generation of XOR function. Twelve state-of-theart 1-bit full adders and one proposed full adder are simulated with HSPICE using 0.18µm CMOS Technology at 1.8V supply voltage. By optimizing the transistor size in each stage the power and delay are minimized. The results of post-layout simulation compared to similar reported ones illustrate significant improvement. Simulation results show great improvement in terms of Power-Delay-Product (PDP). The power consumption of this adder is 200nw.
- **Design of Robust, Energy-Efficient Full Adders for Deep-Submicrometer Design Using Hybrid-CMOS Logic Style Sumeer Goel, Student Member, IEEE, Ashok Kumar, Senior Member, IEEE, and Magdy A. Bayoumi, Fellow**-We present a new design for a 1-b full adder featuring hybrid-CMOS design style. The quest to achieve a good-drivability, noise-robustness, and low-energy operations for deep submicrometer guided our research to explore hybrid-CMOS style design. Hybrid-CMOS design style utilizes various CMOS logic style circuits to build new full adders with desired performance. This provides the designer a higher degree of design freedom to target a

wide range of applications, thus significantly reducing design efforts. We also classify hybrid-CMOS full adders into three broad categories based upon their structure. Using this categorization, many full-adder designs can be conceived. We will present a new full-adder design belonging to one of the proposed categories. The new full adder is based on a novel XOR–XNOR circuit that generates XOR and XNOR full-swing outputs simultaneously. This circuit outperforms its counterparts showing 5%–37% improvement in the power-delay product (PDP). A novel hybrid-CMOS output stage that exploits the simultaneous XOR–XNOR signals is also proposed. This output stage provides good driving capability enabling cascading of adders without the need of buffer insertion between cascaded stages. There is approximately a 40% reduction in PDP when compared to its best counterpart. During our experimentations, we found out that many of the previously reported adders suffered from the problems of low swing and high noise when operated at low supply voltages. The proposed full adder is energy efficient and outperforms several standard full adders without trading off driving capability and reliability. The new full-adder circuit successfully operates at low voltages with excellent signal integrity and driving capability. To evaluate the performance of the new full adder in a real circuit, we embedded it in a 4- and 8-b, 4-operand carry-save array adder with final carry-propagate adder. The new adder displayed better performance as compared to the standard full adders.

- **Design and Analysis of Low-Power 10-Transistor Full Adders Using Novel XOR–XNOR Gates Hung Tien Bui, Yuke Wang, and Yingtao Jiang, Member, IEEE** -Full adders are important components in applications such as digital signal processors (DSP) architectures and microprocessors. In this paper, we propose a technique to build a total of 41 new 10-transistor full adders using novel XOR and XNOR gates in combination with existing ones. We have done over 10 000 HSPICE simulation runs of all the different adders in different input patterns, frequencies, and load capacitances. Almost all those new adders consume less power in high frequencies, while three new adders consistently consume on average 10% less power and have higher speed compared with the previous 10-transistor full adder and the conventional 28-transistor CMOS adder. One draw back of the new adders is the threshold-voltage loss of the pass transistors.
- **Arithmetic Circuits of Redundant SUT-RNS Somayeh Timarchi and Keivan Navi** -The residue number system (RNS) is suitable for implementing high-speed digital processing devices because it supports parallel, modular, fault-tolerant, and carry-bounded arithmetic. The carry propagation is restricted to inside the modulus. The remaining intramoduli carry propagation limits the speed of arithmetic operation. Therefore, the carry-free property of a redundant arithmetic can be used. In this paper, we discuss a recently proposed class of high-radix redundant RNS based on the stored-unibit-transfer representation for modulo 2n + 1 that improves the power-delay-product performance of conventional redundant RNS. In addition, subtraction and multiplication circuits are designed in the proposed system

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